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DEPARTMENT OF ELECTRICAL AND COMPUTER EGINEERING AMERICAN UNIVERSITY OF BEIRUT

FALL TERM 2004-2005
MIDTERM II

EE/CCE 2007

## EECE320 - DIGITAL SYTEMS DESIGN

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NAME: $\qquad$ ID: $\qquad$
COURSE SECTION: SECTION 1 (PROF. CHEHAB)
SECTION 2 (PROF. MANSOUR)

## INSTRUCTIONS:

- THE EXAM IS CLOSED BOOK/CLOSED NOTES. THE DURATION IS TWO HOURS.
- CALCULATORS ARE NOT ALLOWED.
- WRITE YOUR NAME AND ID NUMBER IN THE SPACE PROVIDED ABOVE.
- INDICATE THE SECTION YOU ARE REGISTERED IN.
- PROVIDE YOUR ANSWERS IN THE SPACE PROVIDED ON THE QUESTION SHEET.
- THE SCRATCH BOOKLET WILL NOT BE CONSIDERED IN GRADING.
- BE AS NEAT AND CLEAR AS POSSIBLE.
- ALL QUESTIONS ARE EQUALLY WEIGHTED

| Problem | Total Points | Earned Points |
| :---: | :---: | :---: |
| 1 | 10 |  |
| 2 | 10 |  |
| 3 | 10 |  |
| 4 | 10 |  |
| 5 | 10 |  |
| 6 | 10 |  |
| 7 | 10 |  |
| 8 | 10 |  |
| 9 | 10 |  |
| 10 | 100 |  |
| Total |  |  |

## Problem 1: [10 points]

Using a Moore machine with $D$ Flip-Flops, design a sequence detector that would output a $Z=1$ only after detecting the sequence $\mathbf{1 1 0 0 1}$ on its single input X. Call the states S0, S1 etc. (use don't cares for illegal states and use simplest state assignment)
A. Draw the state diagram in the space below. [7 points]
B. Fill as much as needed in the corresponding state and transition tables shown below.

|  | $\mathbf{X}$ |  |  |
| :---: | :---: | :---: | :---: |
| $\mathbf{S}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{Z}$ |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
| $S^{*}$ |  |  |  |


|  | $\mathbf{X}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Q1Q2Q3 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{Z}$ |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

C. The excitation equations are given by: [ $\mathbf{3}$ points]



D1 = $\qquad$ $\mathrm{D} 2=$ $\qquad$ $\mathrm{D} 3=$ $\qquad$
$\qquad$
$\qquad$
$\qquad$

## Problem 2: [10 points]

Consider the function: $\mathrm{F}=\Sigma_{\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}}(0,2,3,5,7,8,10,11,14,15)$
a) What are the prime implicants of F ? [ $\mathbf{2}$ points]
b) What are the essential prime implicants of F? [2 points]
c) What is a minimum SOP expression for F ? [ $\mathbf{3}$ points]
d) What is a minimum POS expression for F ? [ $\mathbf{3}$ points]


## Problem 3: [10 points]

Consider the Boolean function $\mathrm{F}=\Sigma_{\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}}(1,3,4,11,12,13,14,15)$
a) Implement $F$ using a 4 -input multiplexer and external gates. Connect $A$ and $B$ to the select lines. [ $\mathbf{5}$ points]
b) Implement F using two 3 -to- 8 decoders with enables, an inverter and OR gates with maximum inputs of 4. [5 points]

## Problem 4: [10 points]

Design an Excess-3 to BCD code converter that gives output code of don't-cares for all invalid input combinations. Complete the table to include for every integer the corresponding BCD code representation.

| EXCESS-3 |  |  |  |  | BCD |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{b}_{\mathbf{3}}$ | $\mathbf{b}_{\mathbf{2}}$ | $\mathbf{b}_{\mathbf{1}}$ | $\mathbf{b}_{\mathbf{0}}$ | $\mathbf{g}_{\mathbf{3}}$ | $\mathbf{g}_{\mathbf{2}}$ | $\mathbf{g}_{\mathbf{1}}$ |  |
| $\mathbf{g}_{\mathbf{0}}$ |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 |  |  |  |  |
| 0 | 0 | 0 | 1 |  |  |  |  |
| 0 | 0 | 1 | 0 |  |  |  |  |
| 0 | 0 | 1 | 1 |  |  |  |  |
| 0 | 1 | 0 | 0 |  |  |  |  |
| 0 | 1 | 0 | 1 |  |  |  |  |
| 0 | 1 | 1 | 0 |  |  |  |  |
| 0 | 1 | 1 | 1 |  |  |  |  |
| 1 | 0 | 0 | 0 |  |  |  |  |
| 1 | 0 | 0 | 1 |  |  |  |  |
| 1 | 0 | 1 | 0 |  |  |  |  |
| 1 | 0 | 1 | 1 |  |  |  |  |
| 1 | 1 | 0 | 0 |  |  |  |  |
| 1 | 1 | 0 | 1 |  |  |  |  |
| 1 | 1 | 1 | 0 |  |  |  |  |
| 1 | 1 | 1 | 1 |  |  |  |  |

We want to design a circuit that performs the above conversion. Write the expressions of $g_{3}, g_{2}, g_{1}$, and $g_{0}$ in terms of $b_{3}, b_{2}, b_{1}$ and $b_{0}$.
g3 = $\qquad$
g2 $=$ $\qquad$
$\mathrm{g} 1=$ $\qquad$
g0 $=$ $\qquad$

## Problem 5: [10 points]

A sequential circuit has 2 flip-flops A and B, one input X and one output Y . Its state diagram is shown below. Design the circuit using D flip-flops and draw the corresponding logic diagram.


## Problem 6: [10 points]

We would like to analyze the following clocked synchronous state machine.

A. Write the next state equations for A and B. [4 points]

$$
\begin{aligned}
& \mathrm{A}^{*}= \\
& \mathrm{B}^{*}= \\
&
\end{aligned}
$$

B. Complete the excitation/transition table, and the state table (use the following state names $\mathrm{A}=00$, $\mathrm{B}=01, \mathrm{C}=11, \mathrm{D}=10)[4$ points $]$

|  | $\mathbf{X}$ |  |
| :---: | :---: | :---: |
| $\mathbf{A B}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| 00 |  |  |
| 01 |  |  |
| 11 |  |  |
| 10 |  |  |
|  | $\mathbf{A *} \mathbf{B}^{*}, \mathbf{Y}$ |  |


|  | $\mathbf{X}$ |  |
| :---: | :---: | :---: |
| $\mathbf{S}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| A |  |  |
| B |  |  |
| C |  |  |
| D |  |  |
|  | $\mathbf{S}^{*}, \mathbf{Y}$ |  |

C. Draw the state diagram. [2 points]

## Problem 7 [ 10 points]

Consider the following Master-Slave JK flip-flop built using SR latches. The S input in the SR latches corresponds to a SET, the R input corresponds to a RESET, and the C input corresponds to ENABLE.
(a) Complete the timing diagram below. [8 points]
(b) Do you see a potential problem in this JK flip-flop? [2 points]



## Problem 8: [10 points]

An $M N$ flip-flop has four operations: clear to 0 , no change, toggle, and set to 1 , when inputs $M$ and $N$ are $00,01,10$, and 11 , respectively.
a) Determine the characteristic equation of an $M N$ flip-flop. [2 points]
b) Design an $M N$ flip-flop using a T flip-flop with enable and extra logic gates. [4 points]
c) Design a $J K$ flip-flop using an $M N$ flip-flop and extra logic gates. [4 points]

## Problem 9: [10 points]

Design a 4-bit Johnson counter using D flip-flops.

## Answer:

## Problem 10: [10 points]

In this problem, we want to design a 3-bit counter using a shift register.
a) Assume the shift register below initially stores $\mathrm{Q}_{3} \mathrm{Q}_{2} \mathrm{Q}_{1}=001$. Modify the shift register by adding extra logic gates so that it implements the state diagram shown on the right. (Hint: write next-state equations for $\mathrm{Q}_{3}, \mathrm{Q}_{2}$, $\mathrm{Q}_{1}$ ).


## Solution:

b) Modify your design in part (a) to include the 000 state.

## Solution:


c) The counter you designed in part (b) is shown below as a black box that produces the sequence $000,001,010$, $100,011,110,111,101$ and then repeats. Describe what you would add to your counter so that it produces the sequence $000,001,010,011,100,101,110,111$ and then repeats.


